MohammadHosein Gholamrezaei

Personal Data

Place and Date of Birth:	Tehran, Iran | Apr 27th 1997
Address:	765 Denali Way 202, Charlottesville, VA, United States
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email:	gholamrezaei.mh@gmail.com, uab9qt@virginia.edu
LinkedIn:	MohamamdHosein Gholamrezaei
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Google Scholar:	MohammadHosein Gholamrezaei
ResearchGate:	Mohammadhosein-Gholamrezaei

Education

Current	Ph.D. in Computer Science
	University of Virginia, Charlottesville, VA, United States
Aug 2023	Advisor: Prof. Kevin Skadron
Aug 2023	M.E. in Computer Engineering
	Chosun University, Gwangju, South Korea
Aug 2021	Thesis: "Hardware Acceleration of Fused-Layer Convolutional Neural Networks via Most-Significant-Digit First Arithmetic" | Advisor: Prof. Jeong-A Lee
Sep 2020	B.E. in Computer Engineering
	Shahid Beheshti University, Tehran,Iran
Sep 2015	Thesis: "Implementation of Radio Amateur Transmitter and Receiver on FPGA Platform" | Advisor: Dr. Dara Rahmati

Affiliation

Current	Research Assistant at University of Virginia, Charlottesville, VA
Sep 2023	*Computer Science Department*
Aug 2023	Research Assistant at Chosun University, Gwangju
Sep 2021	*Computer Systems Laboratory*
Aug 2021	Researcher at Institute For Research in Fundamental Sciences, IPM, Tehran
	High Performance Computing Laboratory
Feb 2019	Website: http://ipm.ac.ir

Research Interests

- Computer Architecture
- Hardware Accelerators
- Processing in Memory

Publications

- [J1] Tooba Arifeen, Saeid Gorgin, **Mohammad Hosein Gholamrezaei**, Abdus Sami Hassan, Milos D Ercegovac, Jeong-A Lee, "Low Latency and High Throughput Pipelined Online Adder for Streaming Inner Product", Available at Springer
  Published Journal of Signal Processing Systems, May 2023
- [J2] Kamyar Givaki, Ahmad Khonsari, **M.H. Gholamrezaei**, Saeid Gorgin, M Hassan Na-

jafi, "A Generalized Residue Number System Design Approach for Ultra-Low Power Arithmetic Circuits Based on Deterministic Bit-streams", Available at IEEE explore
Published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, March 2023

- [C1] Saeid Gorgin, **Mohammadhosein Gholamrezaei**, Danial Javaheri and Jeong-A Lee, "An Energy-Efficient K-means Clustering FPGA Accelerator via Most-Significant Digit First Arithmetic",
Accepeted in the International Conference on Field Programmable Technology (FPT), Dec 2022

- [C2] Karvandi, Mohammad Sina and **Gholamrezaei, MohammadHossein** and Monfared, Saleh Khalaj and Medi, Suorush and Abbassi, Behrooz and Amini, Ali and Mortazavi, Reza and Gorgin, Saeid and Rahmati, Dara and Schwarz, Michael, "HyperDbg: Reinventing Hardware-Assisted Debugging", Available at Arxiv,
Accepeted in the ACM Conference on Computer and Communications Security (CCS), Nov 2022

- [C3] Kamyar Givaki, Ahmad Khonsari, **Mohammad Hossein Gholamrezaei**, Dara Rahmati and Saeid Gorgin, "FIR Filter Architectures Using Accurate Unary Stochastic Computing",
Accepeted in IEEE International Conference on Computer Design (ICCD), Oct 2022

- [C4] Gorgin, S., **Gholamrezaei, M. H.**, Javaheri, D., and Lee, J. A. "kNN-MSDF: A Hardware Accelerator for k-Nearest Neighbors Using Most Significant Digit First Computation",
Accepeted in IEEE International System-on-Chip Conference (SOCC), Sep 2022

- [C5] Gorgin, S., **Gholamrezaei, M. H.**, Javaheri, D., and Lee, J. A. "An Efficient FPGA Implementation of k-Nearest Neighbors via Online Arithmetic", Available at IEEE explore
Published in IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM) , May 2022

- [J3] Kamyar Givaki, Reza Hojabr, **M.H. Gholamrezaei**, Ahmad Khonsari, Saeid Gorgin, Dara Rahmati, and M. Hassan Najafi, "High Performance Deterministic Stochastic Computing Using Residue Number System", Available at IEEE explore
Published in IEEE Design and Test , Jan 2021

- [C6] Kamyar Givaki, Reza Hojabr, M. Hassan Najafi, Ahmad Khonsari, **M. Hossein Gholamrezayi**, Saeid Gorgin, and Dara Rahmati "Using Residue Number Systems to Accelerate Deterministic Bit-stream Multiplication", Avalable at IEEE explore
Published in International Conference on Application-specific Systems, Architectures and Processors (ASAP), July 2019

- [C7] Kamyar Givaki, Reza Hojabr, M Hassan Najafi, Ahmad Khonsari,**M Hossein Gholamrezayi**, Saeid Gorgin, Dara Rahmati "A Generalized Residue Number System Design Approach for Ultra-Low Power Arithmetic Circuits Based on Deterministic Bit-streams",
Submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

Patents

- Najafi, Mohammadhassan, Kamyar Givaki, Seyed Reza Hojabrossadati, **M. H. Gholamrezayi**, Ahmad Khonsari, Saeid Gorgin, and Dara Rahmati. "Method and architecture for accelerating deterministic stochastic computing using residue number system." U.S. Patent Application 17/166,378, filed August 5, 2021.

Teaching Assistant

Teacher Assistant, Shahid Beheshti University
- Microprocessors and Assembly Language Course, Dr. Dara Rahmati ,

Held TA sessions, Determined and graded computer assignments, Winter 2018

Teacher Assistant, Shahid Beheshti University
- Microprocessors and Assembly Language Course, Dr. Dara Rahmati ,

Held TA sessions, Determined and graded computer assignments, Spring 2019

Co-Teacher Assistant, Shahid Beheshti University
- Real-Time and Embedded Systems Course Dr. Seyed-Hosein Attarzadeh-Niaki ,

Held some TA sessions, Graded some computer assignments, Winter 2019

Teacher Assistant, Shahid Beheshti University
- Digital Design Course, Dr. Dara Rahmati ,

Held TA sessions, Determined and graded computer assignments and final project, Winter 2019

Teacher Assistant, Shahid Beheshti University
- Microprocessors and Assembly Language Course, Dr. Dara Rahmati ,

Held TA sessions, Determined and graded computer assignments, Spring 2020

Co-Teacher Assistant, Shahid Beheshti University
- Real-Time and Embedded Systems Course Dr. Seyed-Hosein Attarzadeh-Niaki ,

Held some TA sessions, Graded some computer assignments, Winter 2020

Notable Projects

- **HyperDbg**
  - HyperDbg debugger is an open-source, hypervisor-assisted user-mode, and kernel-mode Windows debugger with a focus on using modern hardware technologies. It is a a debugger designed for analyzing, fuzzing and reversing.
  - One of the main developers of HyperDbg
- **The Archer : The Microarchitecture Analyzer**
  - This tool uses several innovative methods to analyze the features of each instruction and MSRs.
  - Designed and implemented a Linux Kernel Module which brute-forces the values of MSRs and transmits the gathered result via USB connection
- **A Generalized ROM-Less Forward-Converter for Residue Number System**
  - Designed a generalized Forward-Converter for Residue Number System which has 30% less area than the most efficient known serial implementation.
  - Implemented using VHDL and synthesized using Synopsys Design Compiler
- **Implementation of SRAM Layout**
  - Implemented 16x4 SRAM VLSI layout using Cadence Virtuoso as VLSI course final project
- **SHA-256 Hash function Low-cost FPGA Implementation**
  - Implemented SHA-256 Hash Function of FPGA Platform
  - Tested the design using a Python program via serial connection

- **Deep Neural Network (DNN) Processing Element**
  - Designed and implemented the Processing Element(PE) for various arithmetic methods based on Eyeriss PE
  - Evaluated performance of each design using Synopsys Design Compiler
- **Fast Fourier Transform(FFT)**
  - Designed and implemented for various arithmetic methods
  - Evaluated performance of each design using Synopsys Design Compiler
- **Oscilloscope Implementation on FPGA**
  - Designed and implemented a simple digital oscilloscope
  - Designed and implemented VGA controller
- **ColorFill Game GUI and AI Implemenation on FPGA**
  - Implemented AI of ColorFill Agent which used BFS algorithm to solve the problem
  - Displayed game environment via VGA interface
- **PaperSoccer Game AI implementation on FPGA**
  - Implemented AI agent of PaperSoccer game on DE-2 FPGA board using LegUp High Level Synthesis Tool
- **Pitch Detection Algorithm using AVR microcontroller**
  - Implemented the auto-correlation algorithms on ATmega32 AVR microcontroller to compute pitch of input audio signal as Microprocessors and Assembly course final project
- **FPGA Implementation of pipelined MIPS processor in Xilinx ISE**
  - Implemented 5-stage piplined version of MIPS processor in Verilog
  - Synthesized and Evaluated HDL Codes using Xilix ISE
- **Messenger**
  - Designed a minimal chat platform using JavaFX (for Advanced Programming course).

Scholarships and Awards

June. 2021	Research Assistant Scholarship , **Chosun University**
Feb. 2020	Candidate For Best Bachelor Thesis Award, **Shahid Beheshti University**
Aug. 2015	Top 1%, The Nationwide Entrance Exam of Iranian Universities (among more than 180,000 contestants)

Languages

Persian:	Mothertongue
English:	Professional working proficiency

Skills

Programming Skills:	Advanced: RTL Design, Microcontrollers Programming Intermediate: High Level Synthesis(HLS), Compiler Design

Programming Languages:	Advanced: VHDL, Scala/Chisel, (System) Verilog, C/C++, Java Intermediate: Python, x86 Assembly,AVR Assembly, ARM Assmebly, Matlab, LaTeX Basic: Javascript
Platform and Tools:	Advanced: Modelsim, Proteus, Atmel Studio, Arduino IDE Intermediate: Xilinx Vivado, Xilinx ISE, Git, QT, Linux, Zynq Synopsys Design Compiler, LegUp, Keil, HAL Library CMSIS Library Visual Studio, Simulink, Microsoft Office Basic: Gem-5, OpenMP, IntelQuartus, Bash Scripting Cadence Virtuoso, Platform IO, LLVM, ANTLR

Selected Courses

Course	Grade(out of 20)
Microprocessors and Assembly Language	20
Real-time and Embedded Systems	20
Computer Aided Design Lab	20
Microprocessors Lab	19.75
Operating System Lab	19
Electronics Lab	19

Course	Grade(out of 4.5)
Computer Arithmetic for Machine Learning	4.5
Advanced Artificial Intelligence	4.0

Hobbies

- Playing basketball
- Movies and TV shows
- Video games
- Swimming
- Electronics fun projects

References

Prof. Jeong-a Lee — Computer Engineering Department
Chosun Univeristy, Gwangju South Korea
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Dr. Saeid Gorgin — Computer Engineering Department
Chosun Univeristy, Gwangju South Korea
gorgin@chosun.ac.kr

Dr. Dara Rahmati — Computer Science and Engineering Department
Shahid Beheshti University
dara.rahmati@ipm.ir